Realistic Geometry of VTX

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Status of VTX pixel

- As you may know and be worried, VTX pixel has had a “event misalignment” problem.
  Run12-15: 10-20%
  Run16: more serious than former runs.

- Event misalignment has been caused by the four-events buffer (FIFO) in the ALICELHCb readout chips.

- But we don’t yet fully understand why the four-events buffer is faulty working

Implementation of VTX in PHG4

- First I planed to export the VTX pixel in PISA (Geant3, Fortran 77) to PHG4.
- But, after reading through the code 'svx.f', I realized it was a bad idea…
- Then I'm now planning to implement VTX using GDML by referring VTX pixel in PISA.
- GDML (Geometry Description Markup Language, format based on XML)
  - is written by text editors
  - can be converted from a STEP file (CAD output)
  - is drawn by ROOT (+ "`--enable-gdml`").

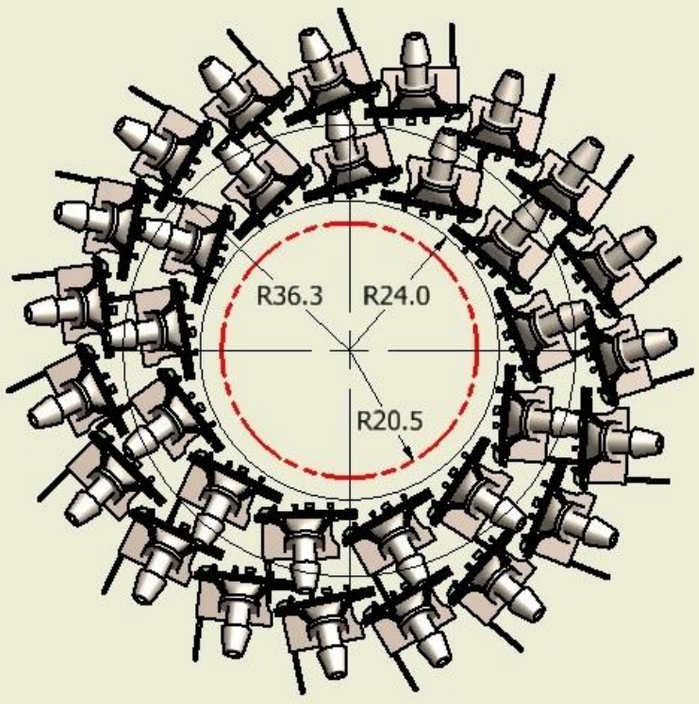
I always use Eclipse.

But needs FASTRAD (shareware).

Rachid's integration plan

Other Options: of P0 and P1 Barrels Integration sPHENIX

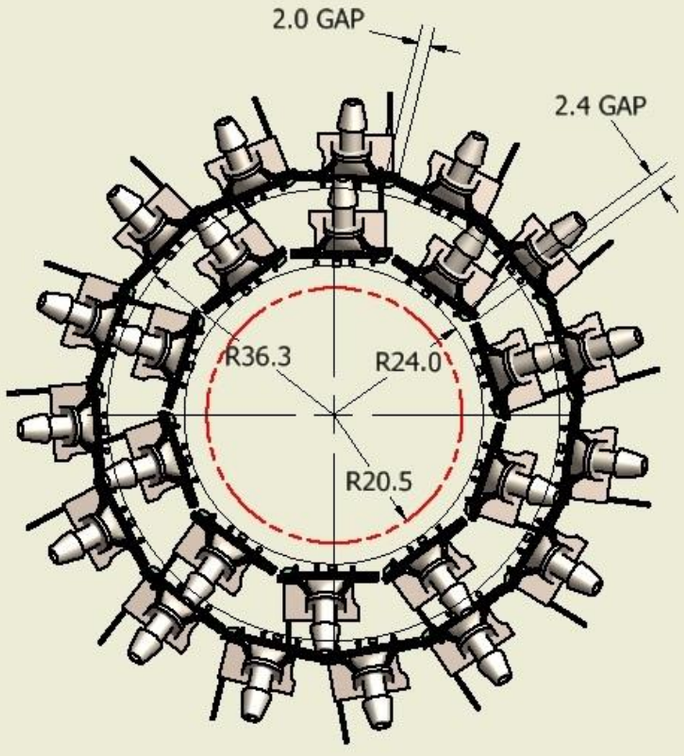
Option (A)



P1 - 19 LADDERS
P0 - 13 LADDERS

32 LADDERS

Option (B)



P1 - 15 LADDERS
P0 - 10 LADDERS

25 LADDERS

Conclusion: P0 and P1 configuration depends on how many good ladders we have (See next slide).

Inventory

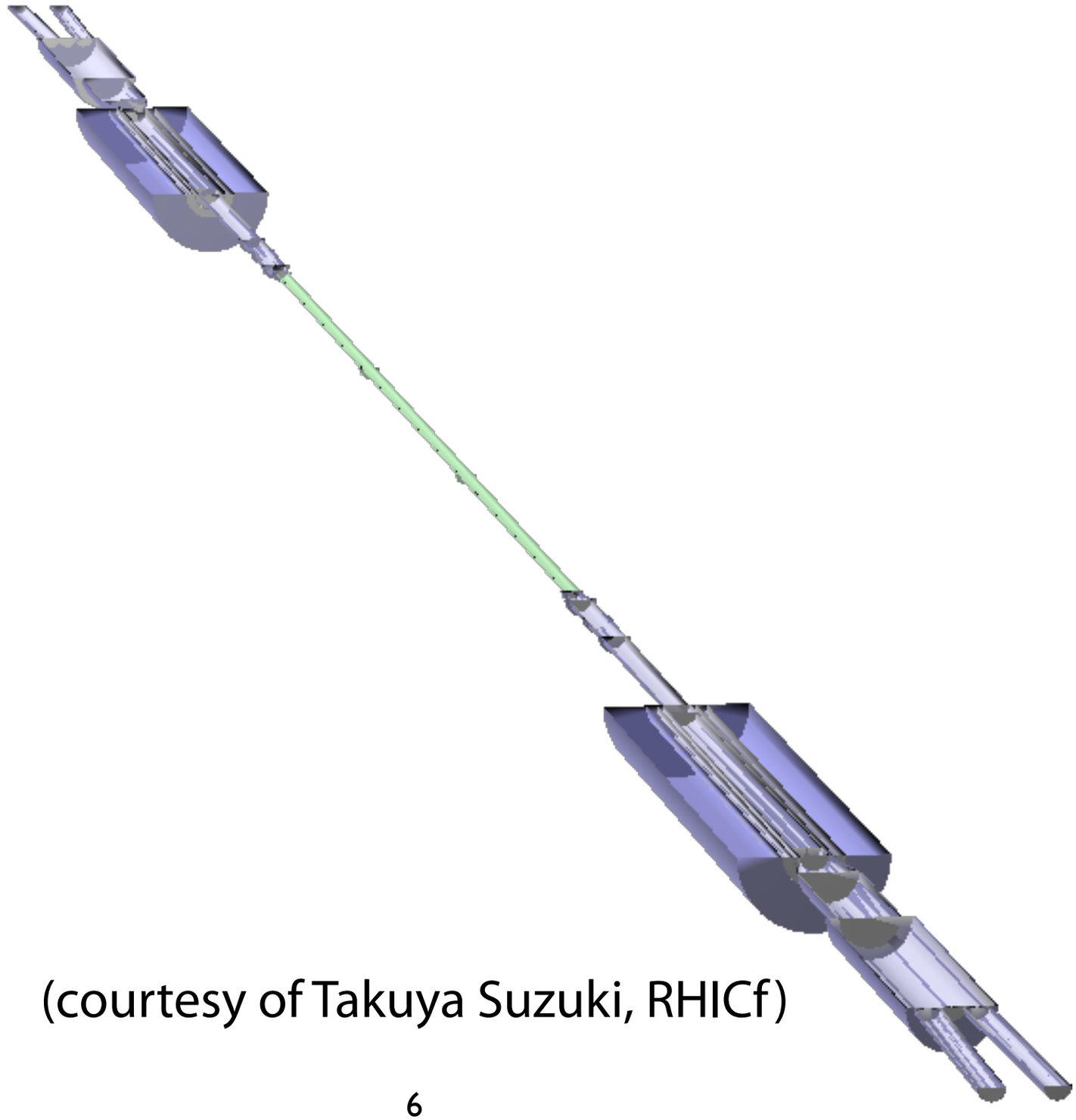
	Ladder ID	Working Pixels (%)	Location		Ladder ID	Working Pixels (%)	Location
01	L43 (new)	94.4	BNL	21	L14 (used)	79.8	BNL
02	L47 (new)	94.4	BNL	22	L16 (used)	79.7	BNL
03	L41 (new)	94.3	RIKEN	23	L35 (used)	79.4	BNL
04	L46 (new)	94.1	RIKEN	24	L5 (used)	78.6	BNL
05	L44 (new)	94.0	RIKEN	25	L12 (used)	77.4	BNL
06	L45 (new)	93.2	RIKEN	26	L25 (used)	75.3	BNL
07	L24 (used)	93.2	BNL	27	L6 (used)	72.9	BNL
08	L39 (used)	94.9	BNL	28	L34 (used)	72.0	BNL
09	L8 (used)	90.1	BNL	29	L11 (used)	71.8	BNL
10	L17 (used)	89.3	BNL	30	L15 (used)	70.7	BNL
11	L26 (used)	87.4	BNL	31	L18 (used)	69.3	BNL
12	L19 (used)	84.7	BNL	32	L10 (used)	66.1	BNL
13	L36 (used)	84.6	BNL	33	L32 (used)	61.7	BNL
14	L33 (used)	83.4	BNL	34	L27 (used)	44.7	BNL
15	L23 (used)	83.4	BNL	35	L20 (used)	32.6	BNL
16	L31 (used)	83.3	BNL	36	L30 (used)	0.0[a]	BNL
17	L22 (used)	82.9	BNL				
18	L9 (used)	80.8	BNL				
19	L21 (used)	80.4	BNL				
20	L13 (used)	80.4	BNL				

Table 11: Available silicon pixel ladders and location

[a]this is caused by failure in wire bonding and can be repaired after Run-16

(http://www.phenix.bnl.gov/phenix/WWW/publish/rnouicer/VTX/2016_VTX/Technical_Note_Silicon_Pixels_Tracker.pdf)

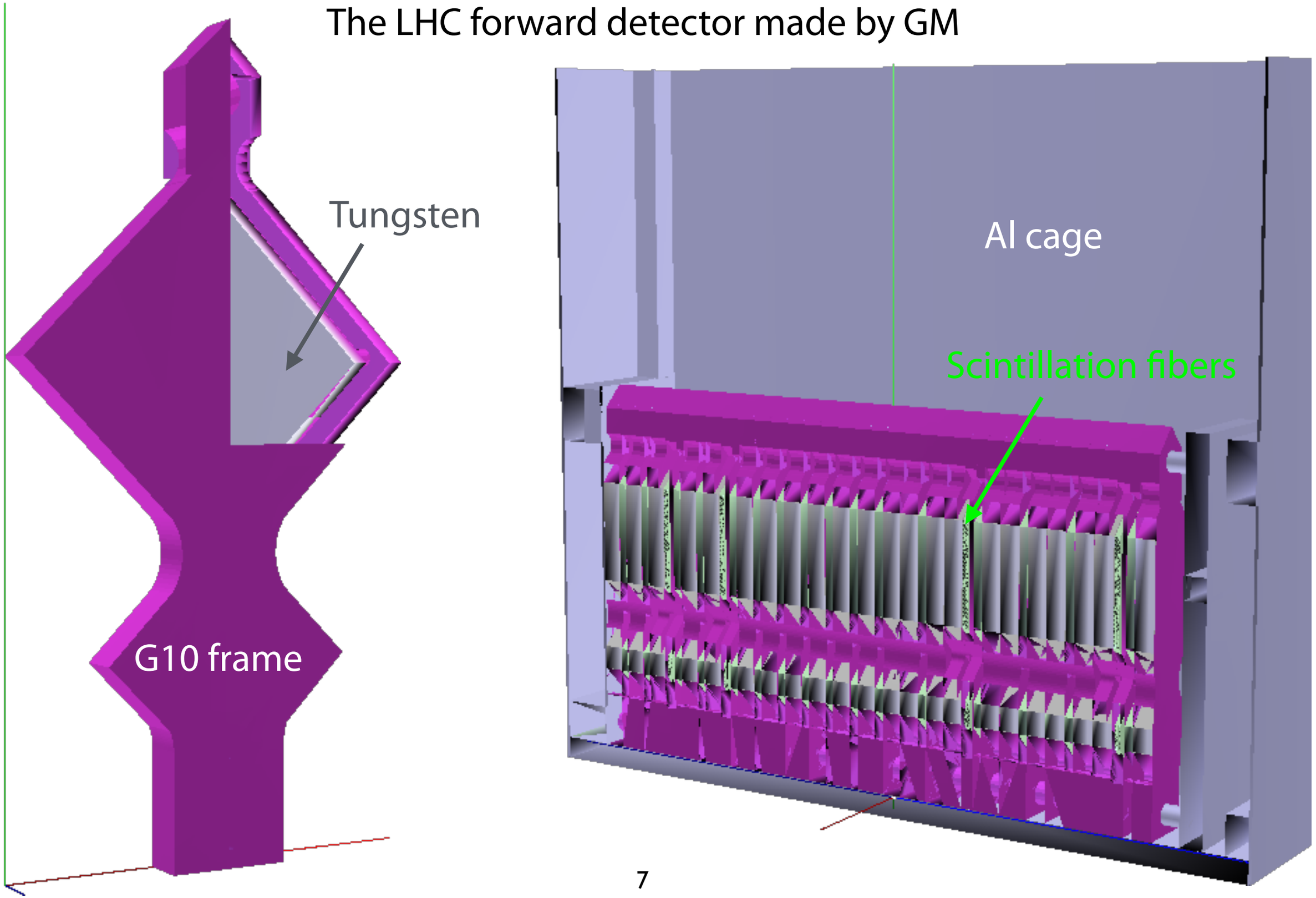
GDML example 1: RHIC beam pipe (STAR)



(courtesy of Takuya Suzuki, RHICf)

GDML example 2: The LHCf detector

The LHC forward detector made by GM



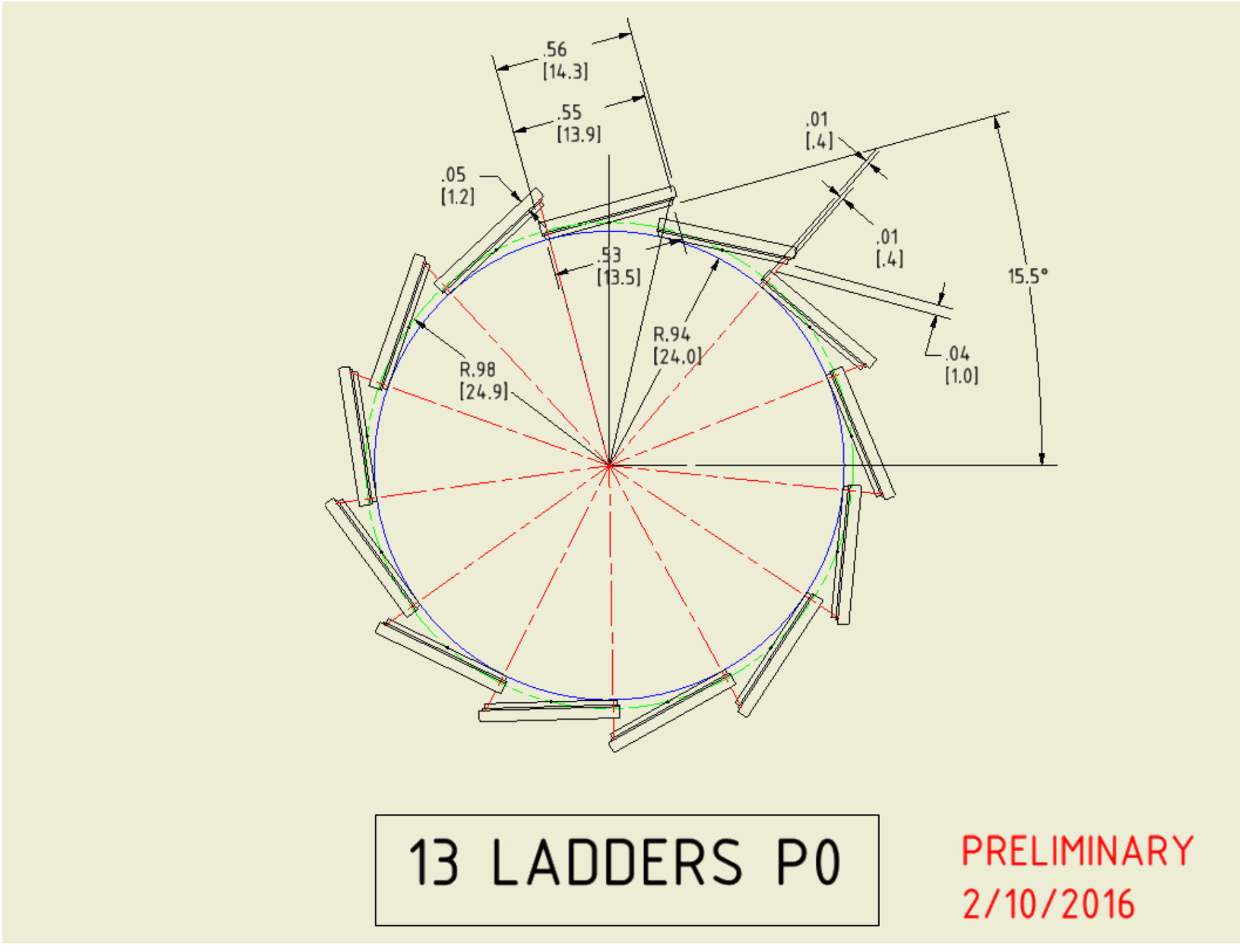
Summary

- I plan to implement VTX in PHG4 using the GDML format;
  - start with simple ladder geometry and then go to small pieces.

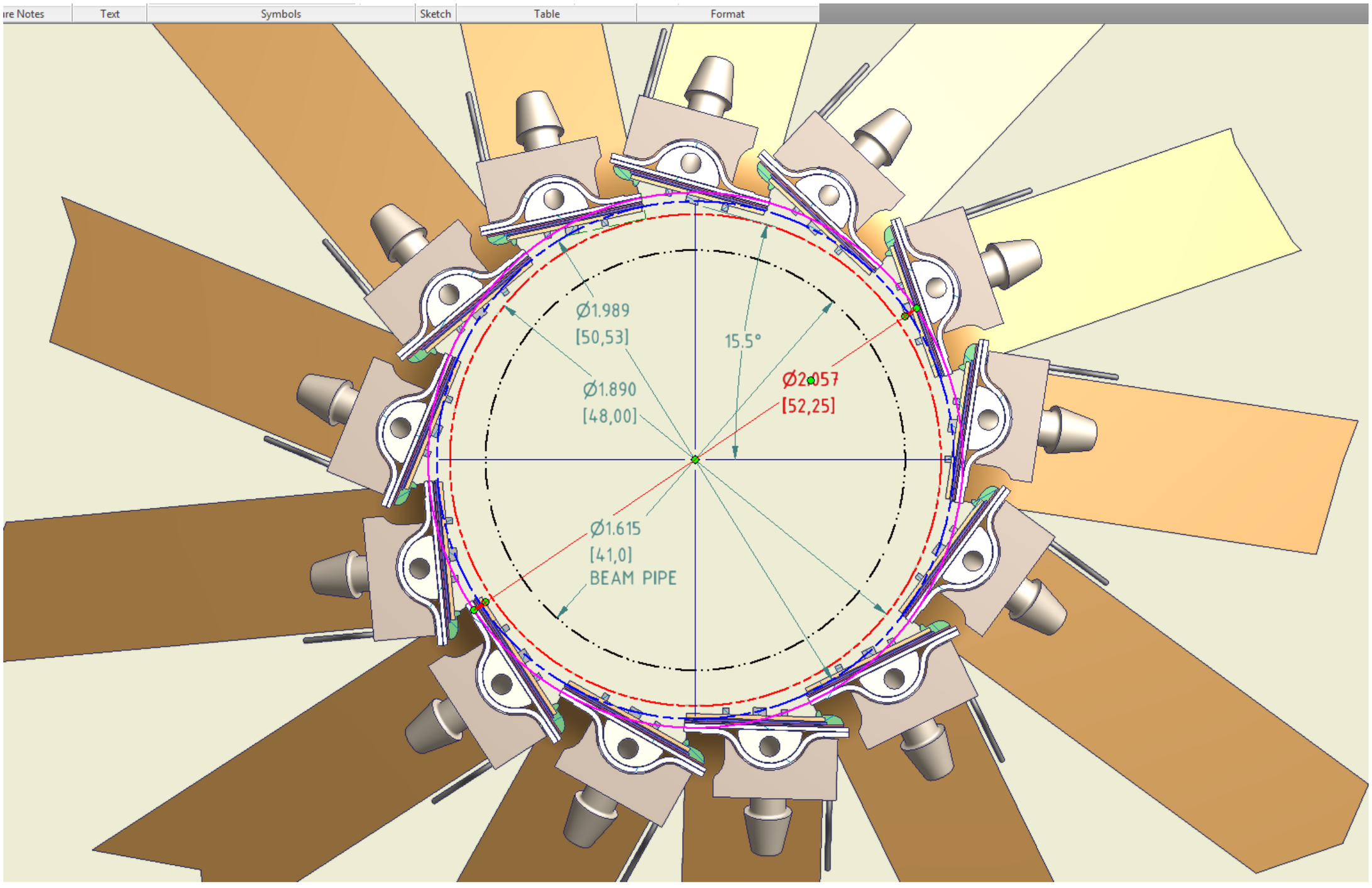
- Simple geometry: 2 weeks
  Detailed geometry (close to Rachid's CAD drawing): 2 or more months.

Backup

➢ How many ladders are needed for P0 to have full coverage in sPHENIX?

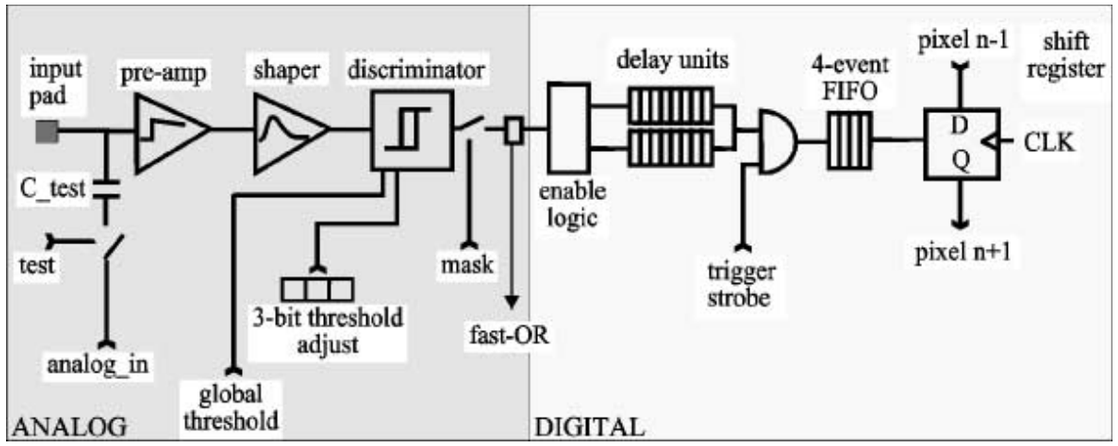


➢ How many ladders are needed for P0 to have full coverage in sPHENIX?

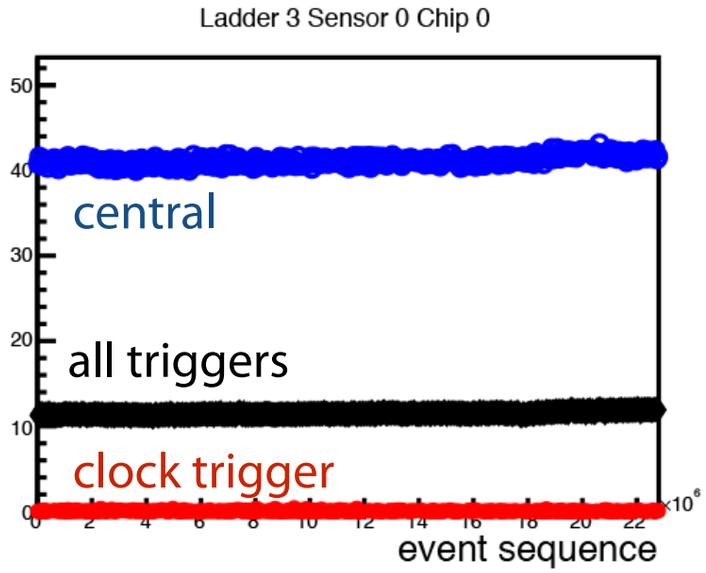


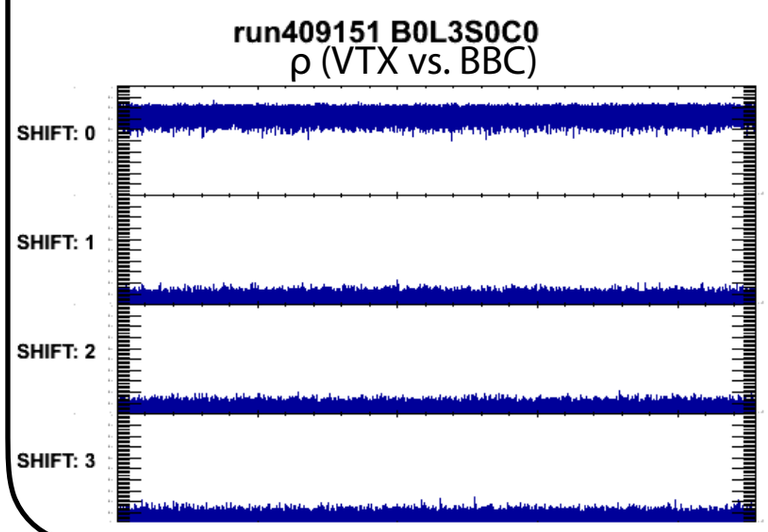
Diagnostic of jump chip

Top: Mean hit rate per chip
Bottom: Correlation coefficient between VTX and BBC (should be ~1) when given numbers of events are artificially shifted.

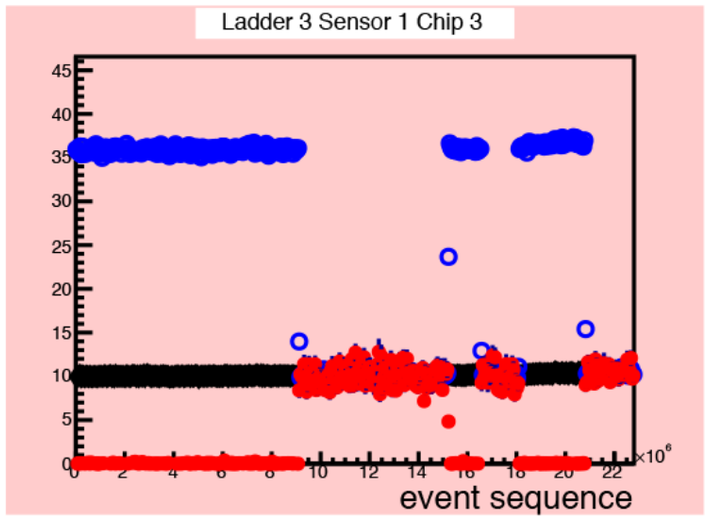


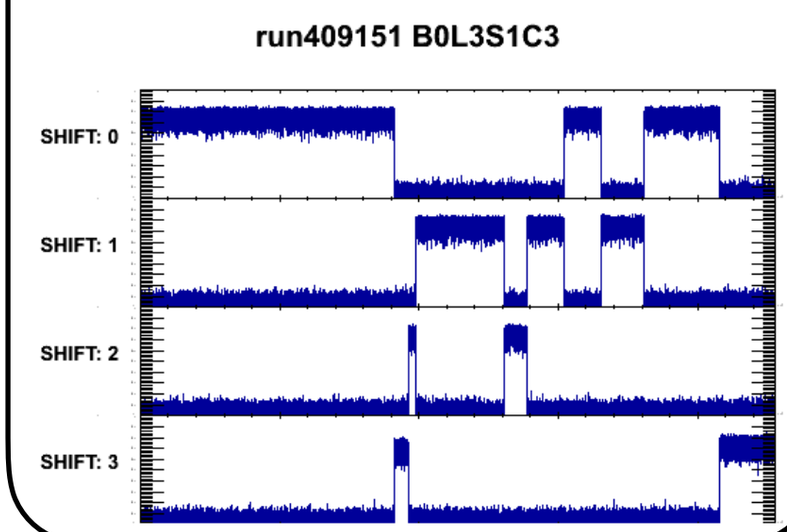
Good chip





Jump chip





Good chip:
SHIFT0 has a good correlation, and the others do not.

Jump chip:
SHIFT0 loses a correlation at the middle of run, and instead SHIFT3 gets a good correlation and moves to SHIFT2 and 1.

→ Are pointers to "a next pushed event" in 4-event buffer faulty working?

(K. Hill, 4/20/2016)